BWCA-Based Dual-Side LCC Compensation Network with Optimized Switching Control Subsystem for High-Efficiency Narrow-Band Dynamic Tuning

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Abstract. Wireless Power Transfer (WPT) has emerged as a promising non-contact charging solution for Electric Vehicles (EVs), offering high safety, convenience, and efficiency. In such systems, the dual-sided LCC compensation network plays a critical role in achieving high power transfer efficiency. However, the performance of inductive power transfer systems is highly sensitive to switching frequency, and conventional LCC designs rely on fixed passive components, making real-time resonance tuning under varying operating conditions difficult. To address this limitation, this paper proposes a novel dynamic tuning strategy by replacing fixed capacitors with Binary Weighted Capacitor Arrays (BWCA) in both the primary and secondary LCC networks. This configuration enables precise, real-time resonance control in response to frequency deviations. MATLAB simulations show that the proposed dual-side LCC network with binary capacitor tuning reaches over 90% efficiency at 12 kW output and 85 kHz operating frequency. When the frequency changes between 81.38 kHz and 90.00 kHz, the system still keeps efficiency above 90% with very little power change, proving strong real-time resonance control.

Keywords: Wireless Power Transfer (WPT); Dual-Sided LCC compensation networks; Dynamic tuning strategy; Binary Weighted Capacitor Arrays (BWCA); Real-time resonance control.

1. Introduction

Wireless Power Transfer (WPT) has emerged as a pivotal non-contact charging solution for Electric Vehicles (EVs), leveraging inherent safety, efficiency, convenience and advantages [1][2]. For mid-range kilowatt-class power transfer, Magnetically Coupled Resonant WPT (MCR-WPT) constitutes the dominant implementation. Crucially, load transients and air gap variations induce nonlinear parametric drift, provoking resonant frequency detuning through impedance mismatch—a phenomenon to which conventional Series–Series (S/S) topologies are highly sensitive [3]. In contrast, the LCC topology offers load-independent constant current/voltage (DC/AC) output, low coupling sensitivity, current-source behavior at the transmitter, and natural soft-switching capability. Experimental validation in a 7.7 kW EV charging scenario confirms 96% peak efficiency from a DC power source with simultaneous ZVS and ZPA operation [4]. Its bilateral design minimizes reactive power through coupling- and load-independent resonance, enabling fixed-frequency operation with strong robustness against resonant frequency fluctuations [5].

The characteristics of the inductive power transfer system are sensitive to the parameters such as switching frequency, coupling coefficient, and component values of the resonant tank [6]. Currently, LCC compensation networks predominantly employ deterministic design methodologies. The resonant elements are analytically optimized and physically fixed under idealized constraints, including nominal mutual inductance, fixed load resistance, and invariant component parameters. This static configuration inherently forfeits frequency adaptability, generating the system operating point to continuously deviate from the preset resonant state, leading to a sharp drop in transmission efficiency, overvoltage of power devices, and even system detuning and oscillation stop [7]. Consequently, the inherent parametric inflexibility of conventional LCC networks, combined with an absence of real-time compensation mechanisms, fundamentally constrains their ability to maintain resonant frequency synchronization under dynamic operating regimes and ultimately undermines transmission efficiency and system stability.

In response to the above, this paper proposes a compensation capacitor tuning method to enhance LCC system robustness under dynamic frequency conditions, specifically targeting the 85kHz operating frequency fluctuations in EV wireless charging. The approach integrates Binary Weighted Capacitor Arrays (BWCA) [8] into a collaborative control structure. By sensing dynamic frequency as input, a switching invocations subsystem generates n-bit binary codes. These codes directly actuate switching circuits of the capacitor bank units, enabling real-time resonant frequency tracking under 85kHz dynamic operating conditions. This frequency-adaptive capability addresses the critical need for dynamic tuning in Dual-Sided LCC networks

2. Method

2.1. Model Dual-Sided LCC Compensation Networks

To overcome the limitations of conventional compensation topologies in achieving both high output power and high efficiency, series–parallel hybrid dual-side LCC compensation networks have been investigated [9]. As shown in Fig.1, the system is supplied by a DC source, followed by an inverter operating at a predefined frequency, a dual-side LCC resonant network, and a full-bridge rectifier that drives the load. The transmitter T-network consists of C_1, C_p, and L_p, while the receiver is symmetrically structured with C_2, C_s, and L_s. The coils L_p and L_s, with equivalent series resistances R_p and R_s, are coupled through mutual inductance M. The input impedance seen from the source is Z_{in}, and the secondary side reflects impedance Z_r to the primary.

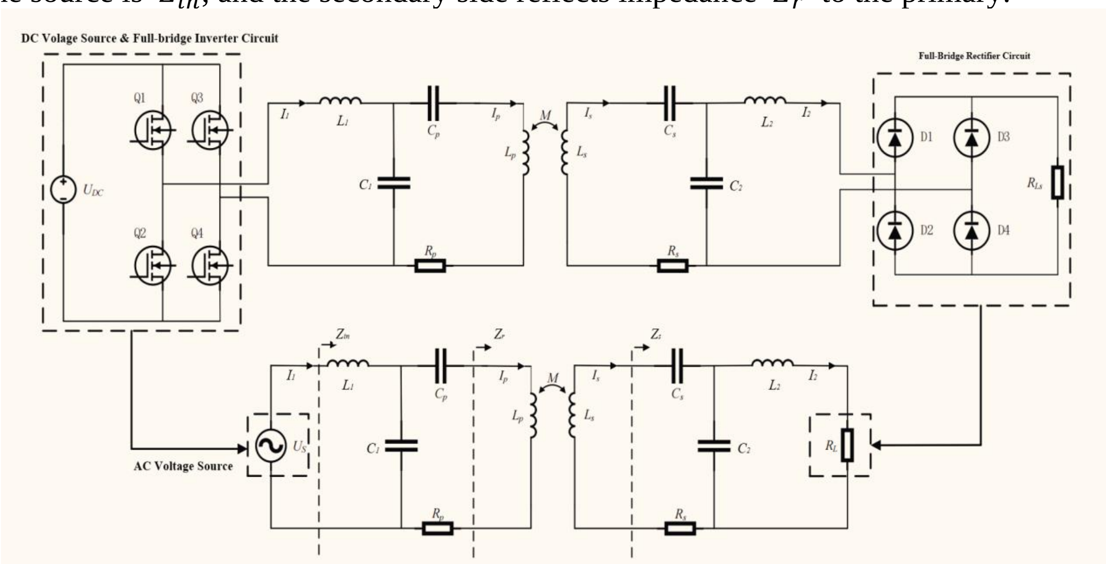

Fig. 1 Topology Structure of Dual-Sided LCC Compensation Networks

From Fig.1, the expressions for Z_{in}, Z_r, Z_s can be calculated as follows:

$$Z_{in} = j\omega L_1 + \frac{\frac{1}{j\omega C_1}\left(j\omega L_p + \frac{1}{j\omega C_p} + R_p + Z_r\right)}{\frac{1}{j\omega C_1} + j\omega L_p + \frac{1}{j\omega C_p} + R_p + Z_r} \tag{1}$$

$$Z_r = \frac{(\omega M)^2}{Z_s} \tag{2}$$

$$Z_s = j\omega L_s + \frac{1}{j\omega C_s} + R_s + \frac{\frac{1}{j\omega C_1}\left(j\omega L_p + R_L\right)}{\frac{1}{j\omega C_1} + j\omega L_p + R_L} \tag{3}$$

By making the above three impedances behave as purely resistive, satisfying the resonance condition. Based on the resonance conditions and the circuit equations, an analytical solution for each circuit parameter can be calculated.

2.2. Design of Key Parameters

2.2.1 Design of Inductance

According to the standard of [10], the operating frequency of the wireless charging system should be limited to the range of 81.38 ~ 90.00 kHz with a center frequency of 85 kHz, and this frequency band will be set as the standard frequency range. Considering the tunability of the system and the ability of band coverage, this paper fixed the static operating frequency to 85 kHz, and carried out the design of the system parameters at this frequency point to adapt the optimal efficiency and power performance.

Since the wireless charging system needs to maintain the resonant state under a fixed structure, to simplify the design,the coil parameters are prioritized and fixed as shown in Table 1.

Table 1. The parameters of transformer

Parameter	Symbol	Value
Primary inductance	L_p	240μH
Secondary inductance	L_s	150μH
Mutual inductance	M	40μH
Coupling coefficient	k	0.211
Primary copper losses	R_p	0.24Ω
Secondary copper loss	R_s	0.20Ω

The series inductors L_1 and L_2 in the matching circuit are designed using the ratios $\alpha_p = \frac{L_p}{L_{rp}}$ and $\alpha_s = \frac{L_s}{L_{rs}}$. Based on system specifications such as minimum power transfer, maximum distance, and tolerance limits, the ratios α_p and α_s must satisfy specific constraints under minimum coupling and inductance conditions [11]. These constraints involve the maximum input voltage $U_{dp,max}$ and minimum output voltage $U_{ds,min}$, which define operational boundaries. Using Eq.4, the values of L_p and L_s were optimized and calculate via MATLAB, yielding α_p and α_s are 8.78 and 2.08, corresponding to measured inductance L_p and L_s values of 27.33 μH and 72 μH respectively.

$$\alpha_s \alpha_p = \frac{\omega \pi^2 P_{omin} \sqrt{L_{p,min} L_{s,min}}}{8 \eta k_{min} U_{ds,min} U_{dp,max}} \tag{4}$$

2.2.2 Design Capacitance of BWCA

The binary-weighted capacitor array (BWCA) enables capacitance adjustment by combining multiple switched capacitor units weighted in powers of two (e.g., 1x, 2x, 4x). To enhance system adaptability under dynamic frequencies, all inductors are fixed and only the four compensation capacitors (C_1, C_p, C_2, C_s) are discretized using BWCAs. This avoids the volume cost of large switch arrays while allowing single-point optimal matching across the entire frequency band. Table 2 and Fig.2 illustrate the resulting capacitance ranges required for each BWCA to maintain resonance across the target frequency band.

Table 2. Range of the four Capacitors

Capacitor	Range of the four capacitors (nF)
C_1	114.474 ~ 139.948
C_p	14.711 ~ 17.985
C_s	40.110 ~ 49.035
C_2	43.453 ~ 53.122

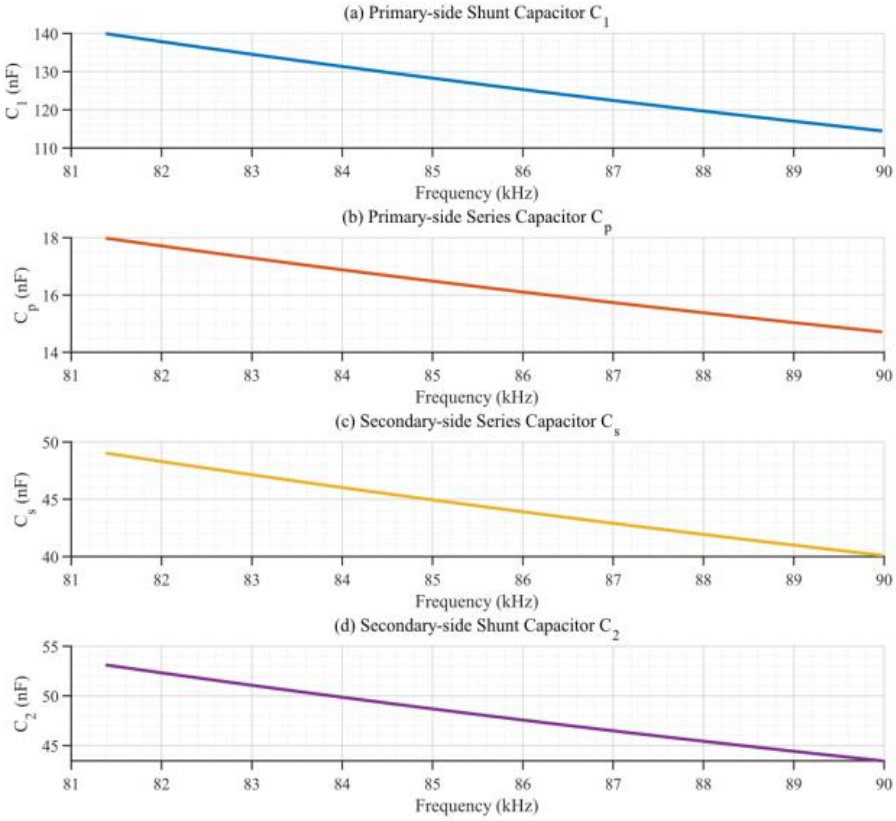

Fig. 2 Calculated Trends of Compensation Capacitors

As shown in Fig.2, the capacitance values exhibit a near-linear decreasing trend because of the narrow operating frequency band. Based on these ranges, the fixed capacitors are replaced with BWCAs. Each BWCA consists of M binary-weighted unit capacitors, covering a dynamic range. Each unit capacitor is controlled by a switch, enabling digital tuning of the total capacitance $\Delta C = C_{max} - C_{min}$. Set the target capacitance C be in the range of demand, and the selected unit capacitance value C_{unit}, minimum digit M, programmable capacitance values C_k needs to be satisfied:

$$\begin{cases} C_{unit} \le \frac{\Delta C}{2} \\ M = \left\lceil log_2\left(\frac{\Delta C}{C_{unit}} + 1\right)\right\rceil \\ C_k = 2^k \cdot C_{unit},\ k = 0,1,2,\dots,M \end{cases} \tag{5}$$

Taking C_1 as an example, a hybrid design with a fixed capacitor and a binary-weighted array is used. The fixed value is set to the minimum required capacitance C_{fixed} is 114.474 nF. The additional variable range required is 25.474 nF. With a chosen unit capacitance C_{unit} of 0.5 nF, the number of bits M is determined by the smallest integer satisfying:

$$(2^M - 1) \cdot C_{unit} \ge \Delta C = 25.474 \tag{6}$$

Substituting the numerical values yields and obtain bit $M = 6$. Since $(2^6 - 1) \cdot 0.5$ nF = 31.5 nF ≥ 25.474 nF. The programmable capacitors are {0.5, 1.0, 2.0, 4.0, 8.0, 16.0} nF. The total capacitance ranges from 114.474 nF (all switches off) to 145.974 nF (all on), covering the required interval. The other three capacitors are designed similarly, and their parameters are summarized in Table 3.

Table 3. Parameters of Capacitor Array

Parameter	C_1	C_p	C_s	C_2
Required Range (nF)	114.474~139.948	14.711~17.985	40.110~49.035	43.453~53.122
ΔC (nF)	25.474	3.274	8.925	9.669
Fixed Capacitor (nF)	114.474	14.711	40.110	43.453
Unit Capacitance (nF)	0.5	0.5	0.5	0.5
Number of Bits (M)	6	3	5	5
Programmable Array Values (nF)	{0.5, 1.0, 2.0, 4.0, 8.0, 16.0}	{0.5, 1.0, 2.0}	{0.5, 1.0, 2.0, 4.0, 8.0}	{0.5, 1.0, 2.0, 4.0, 8.0}
Max Programmable (nF)	31.5	3.5	15.5	15.5
Design Margin (nF)	114.474	14.711	40.110	43.453
Resolution (nF)	0.5	0.5	0.5	0.5

Fig.3 compares the discrete approximation (parameters in Table.2) and continuous solution (parameters in Table.1), illustrating the efficacy of the discretization.

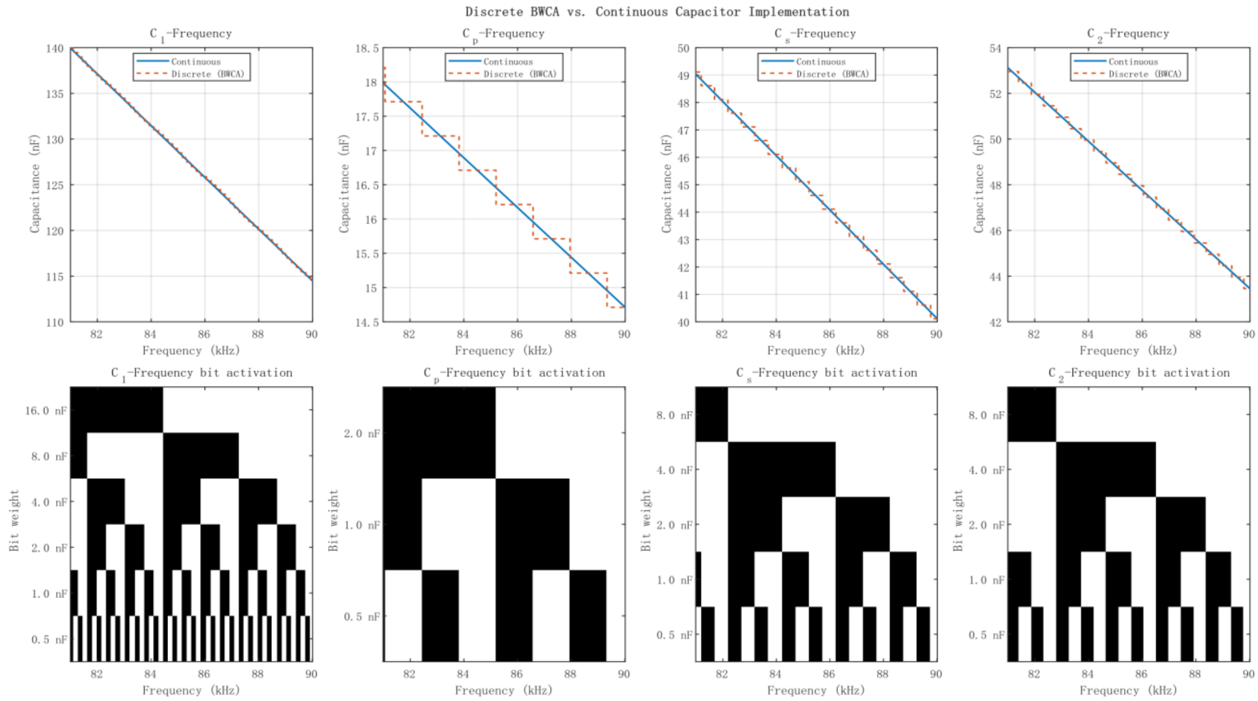

Fig. 3 Comparison of the discrete fit with the continuous solution

2.3. Optimized Switching Control Subsystem

After obtaining the parameters of capacitor array, a control sub-system is designed to map the operating frequency to a binary switching vector. The sub-system takes the instantaneous frequency as input and outputs four binary code vectors:

$$\boldsymbol{S}(f) = [s_1(f), s_2(f), s_3(f), s_4(f)] \tag{7}$$

Among this, $s_1(f)$ is a column vector of 1×6, $s_2(f)$ is a column vector of 1×3, $s_3(f)$ is a column vector of 1×5, $s_4(f)$ is a column vector of 1×5.

Considering actual device errors and environmental variations, this paper add a correction factor. After the introduction of the correction factor, the call of the switch is judged according to the frequency accepted in real time, in addition, in order to avoid the transient shock caused by the one-time large-scale switching, the progressive switching strategy is adopted, the number of switches is limited to the switch at one time, and the maximum number of switches.

$$N_{max} = [\alpha \cdot N_{total}], \alpha \in [0.2,1.0] \tag{8}$$

The α is dynamic stepping factor, it is a quantity that dynamically and adaptively adjusts to changes in efficiency η as follows:

$$\alpha = min\left\{ 1.0\ , max\left[0.2, 0.5 + 0.3 \cdot \left(\frac{\eta}{0.85}\right)\right] \right\} \tag{9}$$

This adaptive design lets the system use careful tuning (small steps α) when efficiency is low, reducing overshoot, and faster tuning (larger steps α) when operating near the best point, speeding up convergence.

3. Simulation and Result

3.1. Simulink Environment Configuration

The Dual-Sided LCC compensated resonant network is created in Simulink as shown in Fig.4.

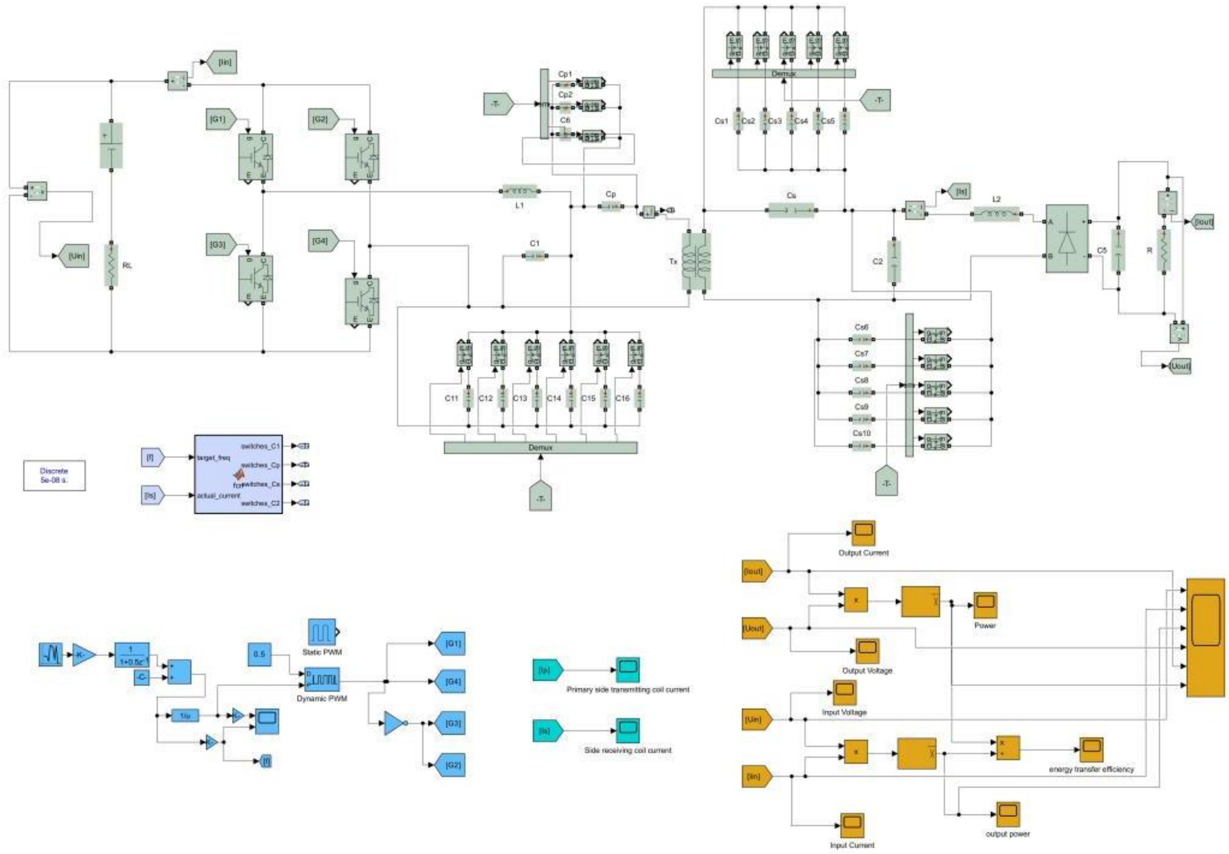

Fig. 4 Model of Dual-Sided LCC Compensation Networks in Simulink

Synthesising the electrical parameters of marketed products, the load is assumed to be 40Ω, DC excitation voltage of 540V.

3.2. Evaluation of System Performance under Static and Dynamic Frequency Conditions

First, the system's operating characteristics are tested at a static working frequency. Following the standard frequency range in [10], three static frequencies (82 kHz, 85 kHz, 88 kHz) are set by adjusting the switching frequency of the full-bridge inverter. This adjustment achieves operation at three distinct frequency points. The three resulting operating states are as follows:

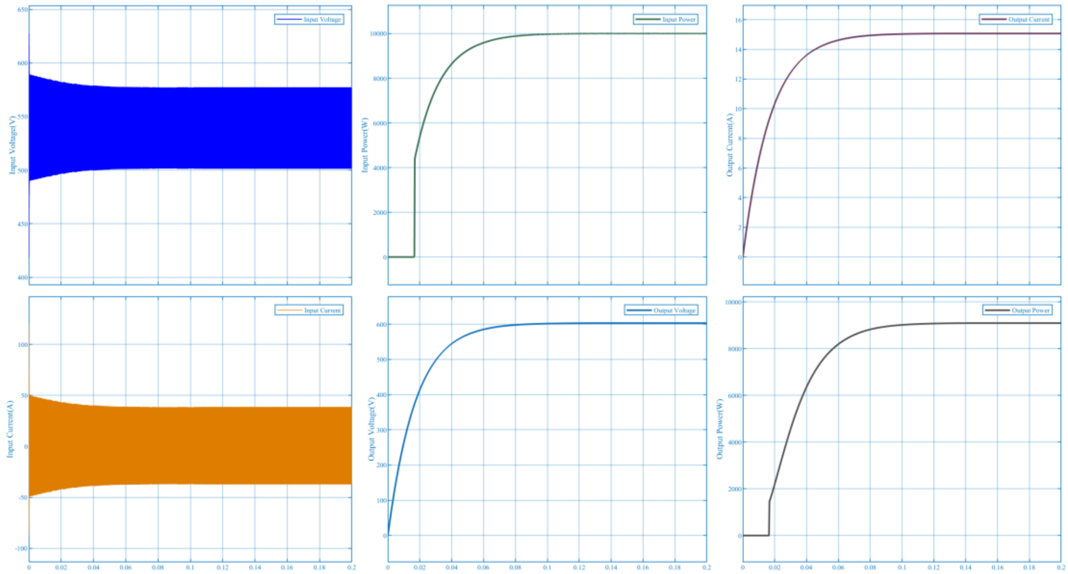

Fig. 5 The state of Static Frequency in 82kHz

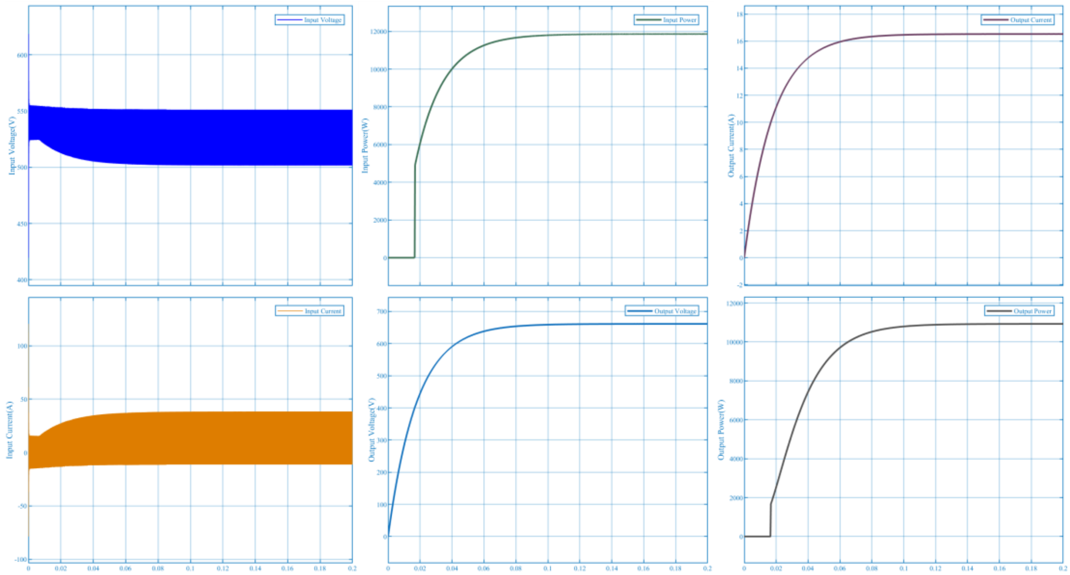

Fig. 6 The state of Static Frequency in 85kHz

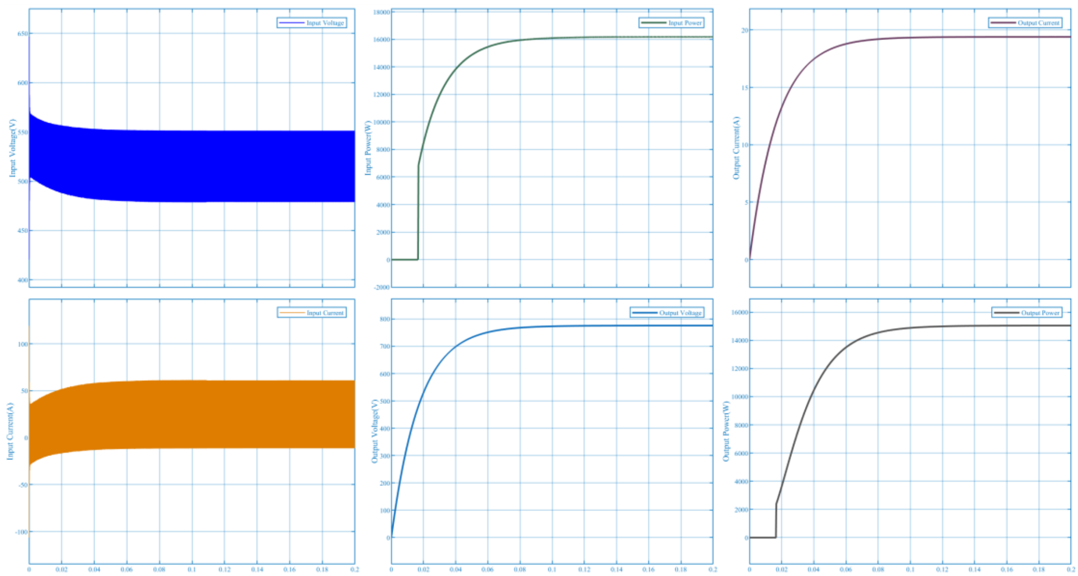

Fig. 7 The state of Static Frequency in 88kHz

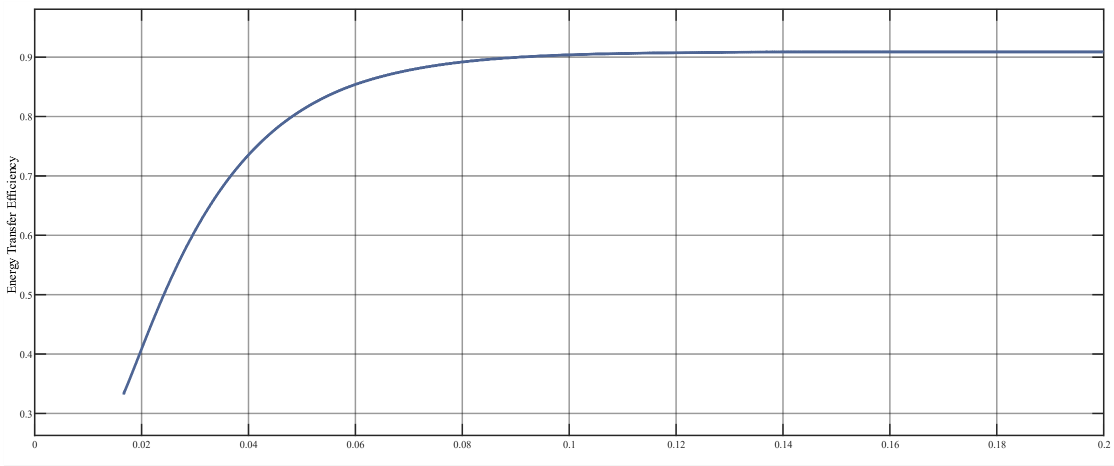

Fig. 8 The Efficiency of Static Frequency in 82kHz

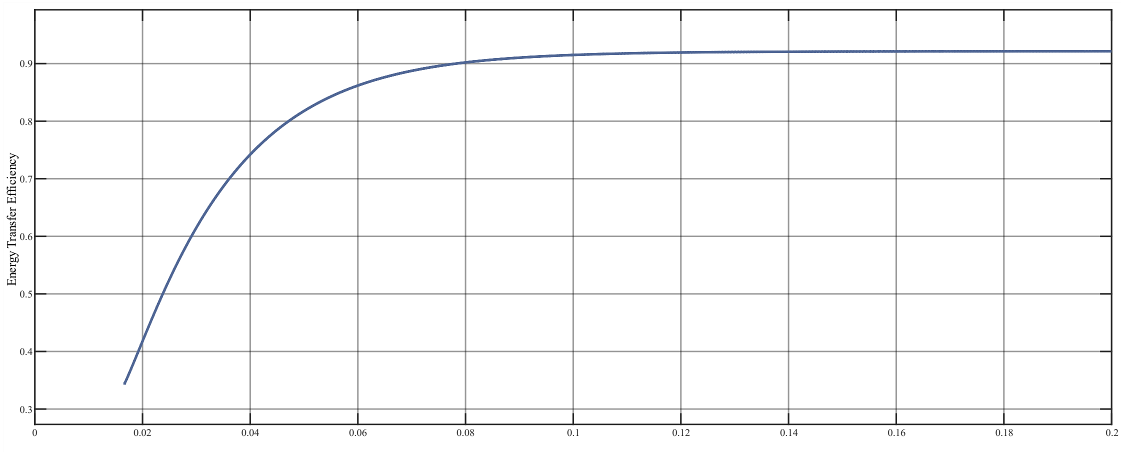

Fig. 9 The Efficiency of Static Frequency in 85kHz

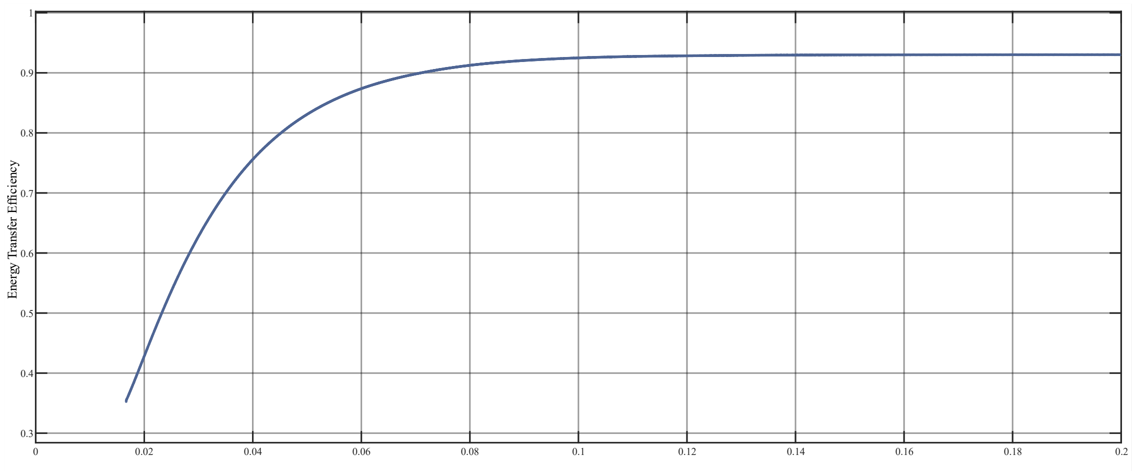

Fig. 10 The Efficiency of Static Frequency in 88kHz

Simulation results (Fig.5-10) indicate that the circuit design exhibits favorable startup and steady-state performance. The output parameters converge rapidly within 80 ms. It is noteworthy that the system maintains stable soft-switching operation at all three tested frequencies (82 kHz, 85 kHz, and 88 kHz), with power transfer efficiency exceeding 90% throughout, reaching a peak value of 92.5% at 85 kHz. Both input and output waveforms demonstrate high stability and low ripple characteristics under steady-state conditions. These findings confirm that the proposed design achieves highly efficient and stable power delivery across the specified frequency range.

The system's resilience to frequency disturbances was further tested by applying random perturbations to the nominal 85 kHz operating frequency. The resulting response, shown in Fig.11:

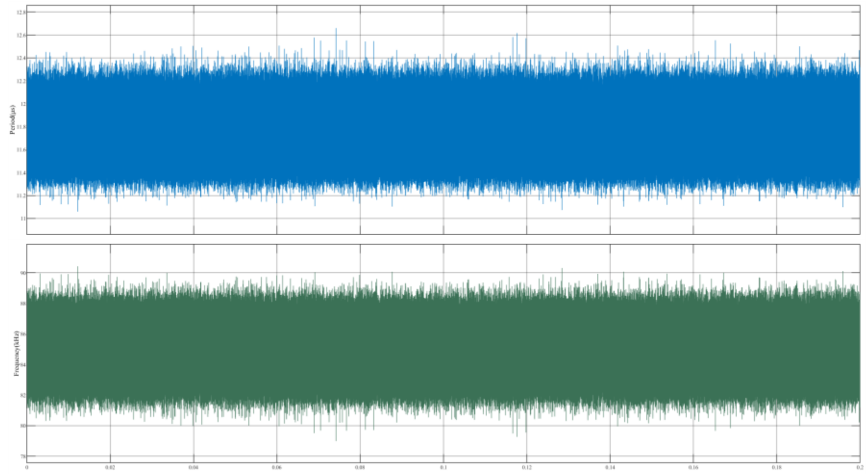

Fig. 11 Dynamic Period / Frequency

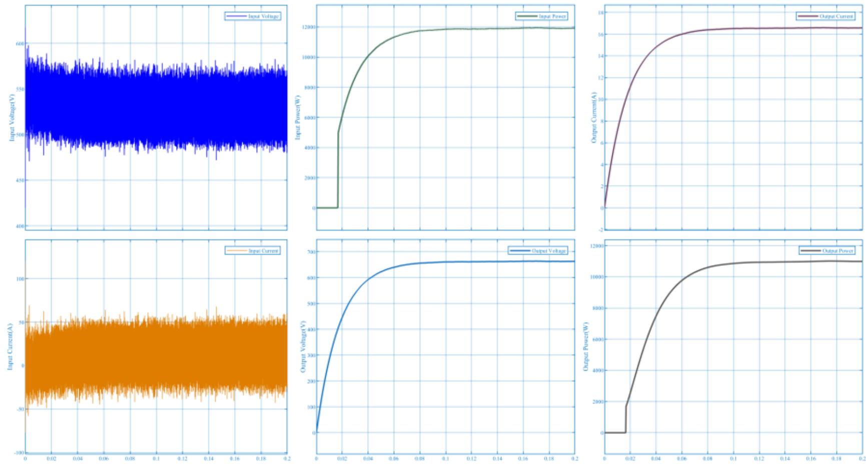

Fig. 12 The state of Dynamic Frequency

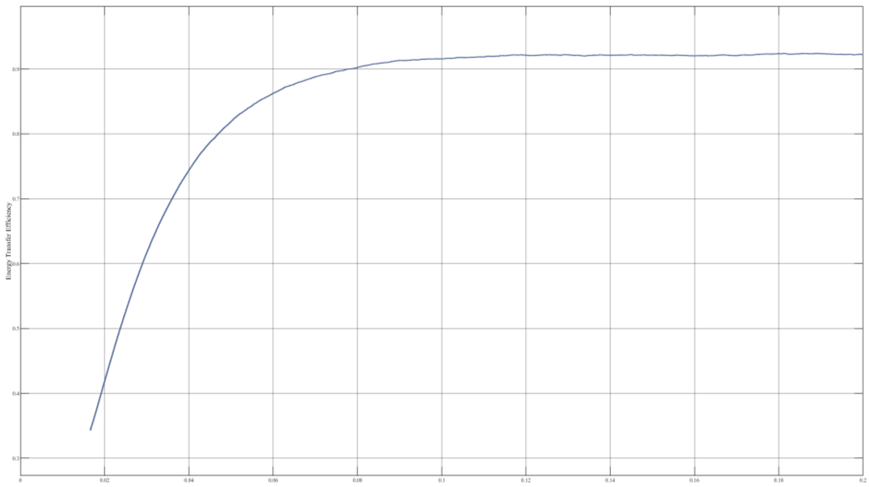

Fig. 13 The Efficiency of Dynamic Frequency

According to the dynamic analysis simulation results (Fig 12 and Fig 13), fluctuations in the inverter switching frequency under dynamic operating conditions introduce unavoidable ripple in the input side. Nevertheless, the system maintains high power output with efficiency exceeding 90%. It should be noted that mild output variability is observed, which stems inherently from the frequency variations and the corresponding adjustment of the capacitor array during dynamic tuning. These variations are part of the intended slow, controlled tuning process and do not result in large-scale or abrupt output instability, furtherly demonstrating the dynamic tuning capability of the current system.

4. Discussion

This study demonstrates that the integration of BWCA with optimized switching control enhances the adaptability and efficiency of a dual-sided LCC compensated WPT system under both static and dynamic conditions. The BWCA allows discrete capacitance adjustment, contributing to consistent resonance maintenance and improved system robustness.

However, several limitations remain. First, the unit capacitance values were selected without accounting for parasitic parameters or variations in transformer and inductor characteristics, potentially affecting practical performance under actual conditions. Second, the fixed capacitance and unit capacitance selection lack an integrated optimization framework. Existing methods also overlook practical constraints such as integer capacitance requirements and manufacturability of non-standard values.

Furthermore, the number of unit capacitors entails a balance between discretization accuracy and physical volume. Increasing unit elements improves tuning resolution but complicates miniaturization. As shows in Fig.3, the current discrete solution approximates the continuous case with good fidelity, yet limitations in switching dynamics persist. The most significant issue is switch-induced delay, arising from both circuit-level soft switching inherent latency and control-level computational complexity in determining switching states.

The system's narrowband nature limits its use across wider frequency ranges. Increasing the bandwidth would need a bigger capacitor array, making the balance between accuracy and size more difficult. Also, parasitic issues in the inductors, especially inductance changes with frequency were not included in the model and need more study. Finally, the control method has not been tested on a compact embedded system, so its real-time performance is still unknown.

5. Conclusion

This work presented a reconfigurable dual-sided LCC compensation network for WPT systems using BWCA and a step-wise switching strategy. The system achieved high efficiency and stability across varying operating conditions through discrete capacitance tuning. Static validation confirmed effective resonance maintenance at target frequencies, while dynamic tests demonstrated robust performance under frequency fluctuations via frequency-tracking and stability-aware switching logic.

The main limitations include switching delays composed of soft-switching circuit delays and computational overhead, and a design that does not yet incorporate parasitic effects or inductor dynamics under frequency variations. The BWCA design also faces inherent compromises between discretization accuracy and physical volume.

Future work will focus on reducing switching delay through hardware and algorithmic improvements, developing a comprehensive optimization framework for capacitance selection, and accounting for parasitic elements in dynamic modeling. Furthermore, efforts will be directed toward implementing the control system on an integrated hardware platform to validate real-time performance and facilitate practical deployment.

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